

1 What is claimed is:

2 1. A method for fabricating wafer-level chip scale packages, comprising :

3 providing a wafer containing a plurality of chips, the wafer having a surface forming  
4 with a plurality of pads;

5 forming a plurality of sacrificial photoresists on the surface of the wafer, each  
6 sacrificial photoresist having a supporting surface without covering the pads;

7 forming a negative photoresist layer on the surface of the wafer, the negative  
8 photoresist layer covering the sacrificial photoresists;

9 patterning the negative photoresist layer to form a plurality of dielectric supporting  
10 bars, the dielectric supporting bars being formed on the supporting surfaces of  
11 sacrificial photoresists;

12 forming a plurality of metal bars on the dielectric supporting bars, the metal bars being  
13 bonded on the dielectric supporting bars and connecting to the pads to assemble a  
14 plurality of pin terminals; and

15 removing the sacrificial photoresists.

16 2. The method for fabricating wafer-level chip scale packages according to claim 1,  
17 wherein the negative photoresist layer on the supporting surfaces of the sacrificial  
18 photoresists has a thickness between  $25\ \mu\text{m}$  and  $250\ \mu\text{m}$ .

19 3. The method for fabricating wafer-level chip scale packages according to claim 1,  
20 wherein the supporting surfaces of the sacrificial photoresists are slanted from the  
21 surface of the wafer.

22 4. The method for fabricating wafer-level chip scale packages according to claim 1,  
23 wherein the sacrificial photoresists are made from the material selected from a positive  
24 photoresist and a positive dry film.

25 5. The method for fabricating wafer-level chip scale packages according to claim 1,  
26 wherein the negative photoresist layer is formed by printing or spin coating.

27 6. The method for fabricating wafer-level chip scale packages according to claim 1,

1        wherein the metal bars are formed by plating, evaporation or sputtering.  
2        7. The method for fabricating wafer-level chip scale packages according to claim 1,  
3        further comprising a step of singulating the wafer to form wafer-level chip scale  
4        packages including the chips after removing the sacrificial photoresist.

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